


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Norito Umehara, et al. Docket: TIJ-28795  
Serial No.: TBD Examiner: TBD  
Filed: Herewith Art Unit: TBD  
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME

PRELIMINARY AMENDMENT

Assistant Commissioner For Patents  
Washington, D. C. 20231

Sir:

"EXPRESS MAIL" mailing label number
<u>EL645450862US</u> , Date of Deposit: : 25 May 2001.
I hereby certify that the Preliminary Amendment and the accompanying Application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 § CFR 1.10 on the above-mentioned date and is addressed to the Assistant Commissioner of Patents, Box New Applications, Washington, DC 20231.
 Allen B. Kroger

Before examination of the above-identified patent application, please make the following amendments:

IN THE SPECIFICATION:

Replacement pages 2, 3 and 9 are enclosed herewith. Replacement pages 10-11 are enclosed herewith so that the original claims will appear on separate pages.

IN THE CLAIMS:

Please amend claims 1, 3-7 and 10 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction substantially perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

3. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

4. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads have notches between said first region and said second region.

6. (Amended) The semiconductor device according to claim 1 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. (Amended) A method of manufacturing semiconductor devices comprising:

disposing roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

disposing a plurality of conductor wires to electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

10. (Amended) The method of manufacturing semiconductor devices according to claim 7 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

Please add new claims 11-19 as follows:

--11. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

12. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

13. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads have notches between said first region and said second region.

14. (New) The semiconductor device according to claim 2 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the

other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

15. (New) The semiconductor device according to claim 3 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

16. (New) The semiconductor device according to claim 4 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

17. (New) The semiconductor device according to claim 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

18. (New) The method of manufacturing semiconductor devices according to claim 8 further comprising a step wherein, prior to said securing step, testing of said semiconductor

chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

19. (New) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.--

## REMARKS

Entry and favorable action of the claims are earnestly solicited in light of the above amendments.

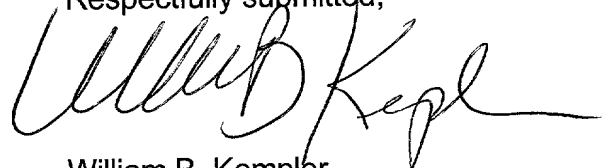
Applicants have amended the claims inter alia to avoid multiple dependent claims and to place the claims in the appropriate form.

Early action on the merits is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current preliminary amendment. The attached page is captioned **"Version with markings to show changes made."**

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

### SUMMARY OF THE INVENTION

The semiconductor device according to one aspect of the present invention comprises: a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip, a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

It is preferable that said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

In addition, it is preferable that said plurality of bonding pads be rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip. Moreover, it is preferable that said plurality of bonding pads be formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

Furthermore, it is preferable that said plurality of bonding pads have notches between said first region and said second region.

In addition, it is preferable that said member be an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of

conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

The method of manufacturing semiconductor devices according to one aspect of the present invention comprises: a step wherein a semiconductor chip upon which is disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and a step wherein a plurality of conductor wires electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

#### **IN THE CLAIMS:**

1. (Amended) A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction substantially perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.



3. (Amended) The semiconductor device according to claim[s] 1 [or 2] wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

4. (Amended) The semiconductor device according to claim[s] 1 [or 2] wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. (Amended) The semiconductor device according to claim[s] 1 [or 2] wherein said plurality of bonding pads have notches between said first region and said second region.

6. (Amended) The semiconductor device according to [any of] claim[s] 1[, 2, 3, 4 or 5] wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. (Amended) A method of manufacturing semiconductor devices comprising:

[a step wherein a semiconductor chip upon which are disposed] disposing roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

[a step wherein] disposing a plurality of conductor wires to electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

10. (Amended) The method of manufacturing semiconductor devices according to [any of claims 7, 8 or 9,] claim 7 further comprising a step wherein, prior to said securing step,

testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

Please add new claims 11-19 as follows:

--11. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

12. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

13. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads have notches between said first region and said second region.

14. (New) The semiconductor device according to claim 2 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

15. (New) The semiconductor device according to claim 3 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

16. (New) The semiconductor device according to claim 4 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

17. (New) The semiconductor device according to claim 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

18. (New) The method of manufacturing semiconductor devices according to claim 8 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

19. (New) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.--

Therefore, an object of the present invention is to provide a structure and method in the wire bonding method that gives adequate connection strength between the bonding pads and conductor wire.

A further object of the present invention is to achieve the previous object while also providing a semiconductor device and its method of manufacture wherein the pitch between bonding pads is made smaller to be suitable to finer pitches.

### SUMMARY OF THE INVENTION

The semiconductor device according to one aspect of the present invention comprises: a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip, a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

It is preferable that said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

In addition, it is preferable that said plurality of bonding pads be rectangular in shape with their short sides lying in a direction along the edges of said semiconductor chip. Moreover, it is preferable that said plurality of bonding pads be formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

Furthermore, it is preferable that said plurality of bonding pads have notches between said first region and said second region.

In addition, it is preferable that said member be an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

The method of manufacturing semiconductor devices according to one aspect of the present invention comprises: a step wherein a semiconductor chip upon which is disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and a step wherein a plurality of conductor wires electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

It is preferable that said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

In addition, it is preferable that said connection step comprises: a first step wherein said first region of said plurality of first bonding pads are connected by conductor wire to said third regions of said plurality of conductors, and a second step wherein said first region of said plurality of second bonding pads are connected by conductor wire to said third regions of said plurality of conductors.

Moreover, it is preferable that said method further comprises a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

the aforementioned QFP, etc., the terminating end of the conductor wire may be bonded to inner leads. In addition, in a semiconductor device containing a plurality of semiconductor chips, the lands may also be the bonding pads of other semiconductor chips.

Moreover, the process of the embodiment illustrated the case in which the bonding to the first pads, namely the bonding pads that have the bonding region on the outside, was first completed and then the bonding to the second pads, namely the bonding pads that have the bounding region on the inside, was performed. However, as long as the present invention is followed, it is also possible to perform bonding of the first pads and second pads alternately starting from the edge of the semiconductor chip. In addition, at the time of working of the present invention, the shape of the bonding pads is not limited to the aforementioned embodiments, but rather they may also be trapezoidal in shape.

#### Effects of the Invention

By means of the present invention as described above, the region of the bonding pad to which the conductor wire is bonded will not be damaged by the contact of probes in the previous inspection step, and accordingly, the reliability of connection of conductor wires to the bonding pads is not decreased.

In addition, according to the present invention wherein the orientation of bonding regions alternates among adjacent bonding pads, it is possible to make the pitch between bonding positions on adjacent bonding pads greater than the pitch between bonding pads, and accordingly, the pitch between bonding pads can be made smaller in spite of the inline layout of bonding pads.

## CLAIMS

1. A semiconductor device comprising:

5 a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for  
10 securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

15 2. The semiconductor device according to claim 1 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

20 3. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are rectangular in shape with their short sides lying in a direction along the edges of said semiconductor chip.

4. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the  
25 direction along the edges of said semiconductor chip.

5. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads have notches between said first region and said second region.

6. The semiconductor device according to any of claims 1, 2, 3, 4 or 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said  
30 external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. A method of manufacturing semiconductor devices comprising:

a step wherein a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

a step wherein a plurality of conductor wires electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

8. The method of manufacturing semiconductor devices according to claim 7 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

9. The method of manufacturing semiconductor devices according to claim 8 wherein said connection step comprises: a first step wherein said first region of said plurality of first bonding pads are connected by conductor wire to said third regions of said plurality of conductors, and a second step wherein said first region of said plurality of second bonding pads are connected by conductor wire to said third regions of said plurality of conductors.

10. The method of manufacturing semiconductor devices according to any of claims 7, 8 or 9, further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.